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EXAMINER
ZHEN, LI B

ART UNIT	PAPER NUMBER
2194	

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12/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/845,606	MICHAELI ET AL.	
	Examiner	Art Unit	
	Li B. Zhen	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,13-15,23,29-43 and 48-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,13-15,23,29-43 and 48-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 3, 13 – 15, 23, 29 – 43 and 48 – 51 are presented for examination.

Response to Arguments

2. Applicant's arguments filed 10/22/2007 have been fully considered but they are not persuasive. In response to the Non-Final Office Action dated 06/21/2007, applicant argues:

> (1) Applicants are trying to cover a queue within a single apparatus, with such application as being used for receiving and distributing packets [p. 8, lines 15 – 26];
>
> (2) Independent claim 23 recites the limitation of "advancing the currently selected one of the plurality of sub-queues to which to add information to a next one of the plurality of the sub-queues to which to add information in a predetermined order among the plurality of sub-queues independent of the stream of information." Gutierrez et al. teaches that the decision on which BUF(0) through BUF(B-1) is selected is based on the stream of information (i.e., to what virtual circuit it belong) [p. 10, lines 18 – 25];
>
> (3) Gutierrez et al. neither teaches or suggests maintaining a same order of cells placed into different BUF(0) through BUF(B- 1) buffers, nor provides a mechanism to advance the currently selected sub-queues independent of the stream of packets. Just because an ordering of cells within a virtual circuit are maintained, does not mean that the order of cells added to a queue by distributed

these cells among a plurality of sub-queues is maintained when they are retrieved [p. 11, lines 5 – 10];

(4) Gutierrez and Parruck are not combinable [p. 11, line 11 – p. 12, line 14].

As to submission (1), examiner acknowledges that the claims recite a queue within a single apparatus for receiving and distributing packets. However, examiner also notes that Gutierrez also discloses a single apparatus [switching node; col. 3, line 55 – col. 4, line 24] with a queue [buffer store 63; col. 21, lines 54 – 67], distributor [input port controls; col. 28, lines 40 – 49], receiver [output port control 72; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39], and receiving and distributed packets [see rejection to the claims below].

In response to argument (2), examiner respectfully disagrees. Although Gutierrez discloses associating a virtual circuit with a buffer, the cells for the virtual circuits are transmitted on a round-robin basis, in order of virtual circuit identifier [col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39]. The virtual circuit identifier determines the next buffer to select [i.e. selecting the buffer that is associated with the virtual circuit]. The selection of the next circuit identifier is on a round-robin basis; thus, the buffers associated with the circuit identifier are also selected on a round-robin basis.

As to argument (3), examiner disagrees and notes that Gutierrez discloses that cells are inserted into the buffer stored on a round-robin basis [col. 3, line 55 – col. 4, line 24], retrieving of cells for all of the virtual circuits transmitted to the buffer store on a round-robin basis, in order of virtual circuit identifier [col. 23, line 33 – col. 24, line 2 and

col. 25, lines 27 – 39] and transferring data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier [col. 28, line 48 – col. 29, line 10 and col. 23, line 33 – col. 24, line 2]. Since each virtual circuit has an associated identifier and buffer, the cells are distributed to different buffers based on the virtual circuit identifier. Gutierrez distributes the cells to its associated buffers in a round-robin order based on the virtual circuit identifier and retrieves the cells from their associated buffers in the same round-robin order based on the virtual circuit identifiers. By inserting and retrieving cells from its associated buffers in a round-robin order based on the virtual circuit identifier, Gutierrez maintains a same order of cells placed in different buffers.

As to argument (4), examiner relied on the Parruck reference to teach queue and sub-queue data structures for distributing data packets and did not suggest modifying the invention Gutierrez to include the features of packet shaping. In addition, the motivation statement is updated to reflect the queue and sub-queue features.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 3, 13 – 15, 29 – 32, 35 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,570,850 to Gutierrez et al. [hereinafter Gutierrez, previously cited].

5. As to claim 1, Gutierrez teaches a line card of a router including a queue [switching nodes 11(n) receive, buffer and forward data received from the computers 11(n) and from other switching nodes 11(n) to facilitate the transfer of data among the computers 12(m); col. 3, line 55 – col. 4, line 24], the queue comprising:

a distributor [input port controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49];

one or more storage elements [buffer store 63 for buffering; col. 21, lines 54 – 67] for storing a data structure [buffer store 63 comprises a plurality of "B" buffers BUF(0) through BUF(B-1); col. 22, lines 1 - 22], the data structure including a plurality of sub-data structures [one buffer BUF(b) associated with the linked list; col. 22, lines 42 – 60] with each of said sub-data structures capable of storing a plurality of stored items of a plurality of items [Each of the buffers BUF(B) can store information from one cell; col. 22, lines 1 – 22]; and

a receiver [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39];

wherein the distributor is configured to distribute the plurality of items to be added to the data structure [input port control 71 transfers the cell to the buffer store 63 for

buffered storage; col. 22, lines 1 – 43] among the plurality of sub-data structures in a predetermined sequence order [input port controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49 and col. 28, line 63 – col. 29, line 10] defined among the plurality of sub-data structures and including each of the plurality of sub-data structures [input port control 71 of an input port 60(i), when it receives a cell associated with a virtual circuit, will need to access (a) the linked list information maintained by the buffer manager 64 for the free list to identify a buffer BUF(b) in the buffer store 63 in which it is to store the cell; col. 28, lines 1 – 40]; and the receiver is configured to receive the items from the plurality of sub-data structures in the sequence order [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis, in order of virtual circuit identifier, as long as there are cells for the respective virtual circuits buffered in the buffer store 63; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39] such that the plurality of items are received by the receiver from the data structure in a first-in the data structure, first-out the data structure order [switching nodes transfer data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10 and col. 23, line 33 – col. 24, line 2].

6. As to claim 13, Gutierrez teaches a line card or a router including a queue [switching nodes 11(n) receive, buffer and forward data received from the computers 11(n) and from other switching nodes 11(n) to facilitate the transfer of data among the computers 12(m); col. 3, line 55 – col. 4, line 24], the queue comprising:

one or more storage elements [buffer store 63 for buffering; col. 21, lines 54 – 67] for storing a plurality of data structures [buffer store 63 comprises a plurality of "B" buffers BUF(0) through BUF(B-1); col. 22, lines 1 - 22], each of the plurality of data structures including a plurality of sub-data structures [one buffer BUF(b) associated with the linked list; col. 22, lines 42 – 60] capable of storing a plurality of stored pieces of a plurality of pieces of information [Each of the buffers BUF(B) can store information from one cell; col. 22, lines 1 – 22];

a storage selector configured to select among the plurality of data structures for a particular piece of the plurality of pieces of information [access (a) the linked list information maintained by the buffer manager 64 for the free list to identify a buffer BUF(b) in the buffer store 63 in which it is to store the cell; col. 28, lines 1 – 40; buffer manager 64 maintains a free list header including a head pointer and a tail pointer for the free list; col. 22, lines 1 – 42];

a distributor [input port controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49]; and

a receiver [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39];

wherein the distributor is configured to distribute each of the plurality of pieces of the information to be added [input port control 71 transfers the cell to the buffer store 63 for buffered storage; col. 22, lines 1 – 43] to a particular one of the plurality of data structures across the plurality of sub-data structures belonging to the particular one of

the plurality of data structures in a predetermined sequence order [input port controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49 and col. 28, line 63 – col. 29, line 10] defined across the plurality of sub-data structures and including each of the plurality of sub-data structures [input port control 71 of an input port 60(i), when it receives a cell associated with a virtual circuit, will need to access (a) the linked list information maintained by the buffer manager 64 for the free list to identify a buffer BUF(b) in the buffer store 63 in which it is to store the cell; col. 28, lines 1 – 40]; and the receiver is configured to receive the items from the plurality of sub-data structures in the sequence order [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis, in order of virtual circuit identifier, as long as there are cells for the respective virtual circuits buffered in the buffer store 63; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39] such that the plurality of pieces of information are received by the receiver from the particular one of the plurality of data structures in a first-in the particular one of the plurality of data structures, first-out the particular one of the plurality of data structures order [switching nodes transfer data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10 and col. 23, line 33 – col. 24, line 2].

7. As to claim 2, Gutierrez teaches each of the sub-data structures includes a linked-list data structure configured for storing items of the plurality of stored items [a

plurality of "B" buffers BUF(0) through BUF(B-1) (generally identified by (BUF(b)), which are organized in linked lists; col. 22, lines 1 – 22].

8. As to claim 3, Gutierrez teaches storage for storing a head and a tail of the linked list data structure of each of the plurality of sub-data structures [pointers to the locations of the head and tail of the linked list; col. 8, line 65 – col. 9, lines 40].

9. As to claim 14, Gutierrez teaches each of the sub-data structures includes a linked-list data structure configured for storing pieces of information of the plurality of pieces of information [a plurality of "B" buffers BUF(0) through BUF(B-1) (generally identified by (BUF(b)), which are organized in linked lists; col. 22, lines 1 – 22].

10. As to claim 15, Gutierrez teaches a storage for storing a head and a tail of the linked list data structure of each of the plurality of sub-data structures [pointers to the locations of the head and tail of the linked list; col. 8, line 65 – col. 9, lines 40].

11. As to claim 29, Gutierrez the sequence order is a round robin order among the plurality of sub-data structures [switching nodes transfer data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39].

12. As to claim 30, Gutierrez teaches the distributor includes a counter configured to identify the sequence order [a buffer count value; col. 22, lines 1 – 42].

13. As to claim 31, Gutierrez teaches the sequence order is a round robin order among the plurality of sub-data structures [switching nodes transfer data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39].

14. As to claim 32, Gutierrez teaches the distributor includes a counter configured to identify the sequence order [buffer count value; col. 22, lines 1 – 42].

15. As to claim 35, Gutierrez teaches the distributor is configured to distribute the plurality of items among the plurality of sub-data structures without regard to the content of items of the plurality of items [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39].

16. As to claim 37, Gutierrez teaches the distributor is configured to said distribute the plurality of pieces of the information among the plurality of sub-data structures without regard to the content of piece of the plurality of pieces of the information [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted

therethrough on a round-robin basis; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39].

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 23, 33, 34, 36 and 38 – 43 and 48 – 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutierrez in view of U.S. Patent No. 7,002,916 to Parruck et al. [hereinafter Parruck, previously cited].

20. As to claim 23, Gutierrez teaches the invention substantially as claimed including a method performed by a single appliance [col. 3, line 55 – col. 4, line 24], the method comprising:

(a) receiving a particular piece of information of a stream of pieces of information to be added to a data structure [input port control 71 transfers the cell to the buffer store 63 for buffered storage; col. 22, lines 1 – 43] with each of capable of storing a plurality of pieces of information in the stream of pieces of information [Each of the buffers BUF(B) can store information from one cell; col. 22, lines 1 – 22];

(b) adding the particular piece of information to a currently selected one of the plurality of sub-data structures to which to add information [input port control 71 of an input port 60(i), when it receives a cell associated with a virtual circuit, will need to access (a) the linked list information maintained by the buffer manager 64 for the free list to identify a buffer BUF(b) in the buffer store 63 in which it is to store the cell; col. 28, lines 1 – 40];

(c) advancing the currently selected one of the plurality of sub-data structure to which to add information to a next one of the plurality of the sub-data structure [an input port 60(i), when it receives a cell associated with a virtual circuit, will need to access (a) the linked list information maintained by the buffer manager 64 for the free list to identify a buffer BUF(b) in the buffer store 63 in which it is to store the cell; col. 28, lines 1 – 40 and col. 22, lines 1 – 42] to which to add information in a predetermined order among the plurality of sub-structure independent of the stream of information [input port

controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49];

(d) removing information from a currently selected one of the plurality of sub-queues to which to remove information [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39];

(e) advancing the currently selected one of the plurality of sub-data structure to which to remove information to a next one of the plurality of sub-data structure [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis, in order of virtual circuit identifier, as long as there are cells for the respective virtual circuits buffered in the buffer store 63; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39] to which to remove information in the predetermined order [switching nodes transfer data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10 and col. 23, line 33 – col. 24, line 2]; and

repeatedly performing steps (a)-(c) to add information to the data structure [col. 28, line 48 – col. 29, line 10] and steps (d)-(e) to remove information from the data structure [on a round-robin basis, in order of virtual circuit identifier, as long as there are cells for the respective virtual circuits buffered in the buffer store 63; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39] such that pieces of information of the stream of pieces of information are added to data structure and removed from the data structure in the same order [switching nodes transfer data from cells received thereby for virtual

circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10 and col. 23, line 33 – col. 24, line 2]. Although Gutierrez teaches the invention substantially, Gutierrez does not specifically teach the data structures and sub-data structures as queues and sub-queues.

However, Parruck teaches receiving a particular piece of information of a stream of pieces of information [VC manager 195 receives all the cells; col. 7, lines 57 – 64] to be added to a queue [queues of queues 200(0) 200(m); col. 7, lines 48 – 58], the queue including a plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58] with each of capable of storing a plurality of pieces of information [data encapsulated in cells or data packets; col. 7, lines 34 – 43] in the stream of pieces of information [VC queue is a queue of cells received; col. 7, lines 47 – 58]; adding the particular piece of information to a currently selected one of the plurality of sub-queues to which to add information [incoming cells are stored in an input buffer; col. 10, lines 7 – 16], add information in a predetermined order among the plurality of sub-queues independent of the stream of information [maintains the order of the VC queues; col. 12, lines 47 – 67], removing information from a currently selected one of the plurality of sub-queues to which to remove information in the predetermined order [col. 12, lines 47 – 67] and repeatedly performing steps to add information to the queue and steps to remove information from the queue [col. 11, lines 17 – 34].

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Gutierrez to include the features of receiving a particular piece of information of a stream of pieces of information to be

added to a queue, the queue including a plurality of sub-queues, add information in a predetermined order among the plurality of sub-queues, and removing information from a currently selected one of the plurality of sub-queues in the predetermined order because the queues provides a data structure for temporarily storing data packets in which the data packets are maintained in a First-In-First-Out order.

21. As to claim 33, Gutierrez as modified teaches a queue for storing items of a stream of information [queues of queues 200(0) 200(m); col. 7, lines 48 – 58 of Parruck] with said items received in a particular order [input port controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49 of Gutierrez], the queue being implemented by a single apparatus [col. 3, line 55 – col. 4, line 24 of Gutierrez], the queue comprising:

a plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58 of Parruck], each of the plurality of sub-queues capable of storing a plurality of items [data encapsulated in cells or data packets; col. 7, lines 34 – 43 of Parruck];

an enqueue distributor configured to receive said items of the stream of information in said particular order [input port controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49 and col. 28, line 63 – col. 29, line 10 of Gutierrez], and configured to distribute said items to the plurality of sub-queues in a predetermined sequence order [input port control 71 of an input port 60(i), when it receives a cell associated with a virtual circuit, will need to access (a) the linked list information maintained by the buffer manager 64 for the free list to identify a

buffer BUF(b) in the buffer store 63 in which it is to store the cell; col. 28, lines 1 – 40 of Gutierrez] among the plurality of sub-queues such that each of said items are only stored in a single one of the plurality of sub-queues [input port control 71 transfers the cell to the buffer store 63 for buffered storage; col. 22, lines 1 – 43 of Gutierrez]; and

a dequeue receiver configured to only receive said items of the stream of information from the plurality of queues in the predetermined sequence order [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis, in order of virtual circuit identifier, as long as there are cells for the respective virtual circuits buffered in the buffer store 63; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39 of Gutierrez] and to forward said items in said particular order [switching nodes transfer data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10 and col. 23, line 33 – col. 24, line 2 of Gutierrez]. As to the motivation for combining Gutierrez and Parruck, see the rejection to claim 23 above.

22. As to claim 48, Gutierrez as modified teaches a queue for storing items of a stream of information [queues of queues 200(0) 200(m); col. 7, lines 48 – 58 of Parruck] with said items received in a particular order [col. 28, lines 40 – 49 of Gutierrez], the queue being implemented by a single apparatus [col. 3, line 55 – col. 4, line 24 of Gutierrez], the queue comprising:

a plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58 of Parruck], each of the plurality of sub-queues capable of storing a plurality of items [data encapsulated in cells or data packets; col. 7, lines 34 – 43 of Parruck];

means for receiving said items of the stream of information in said particular order [input port controls 71 will have the higher priority, on a round-robin basis as among themselves; col. 28, lines 40 – 49 and col. 28, line 63 – col. 29, line 10 of Gutierrez], and for distributing said items to the plurality of sub-queues in a predetermined sequence order [input port control 71 of an input port 60(i), when it receives a cell associated with a virtual circuit, will need to access (a) the linked list information maintained by the buffer manager 64 for the free list to identify a buffer BUF(b) in the buffer store 63 in which it is to store the cell; col. 28, lines 1 – 40 of Gutierrez] among the plurality of sub-queues such that each of said items are only stored in a single one of the plurality of sub-queues [input port control 71 transfers the cell to the buffer store 63 for buffered storage; col. 22, lines 1 – 43 of Gutierrez], wherein items distributed to a sub-queue are stored in the sub-queue [VC queue is a queue of cells received; col. 7, lines 47 – 58 of Parruck]; and

means for retrieving said items of the stream of information from the plurality of queues in the predetermined sequence order [output port control 72 initiates retrievals of cells for all of the virtual circuits transmitted therethrough on a round-robin basis, in order of virtual circuit identifier, as long as there are cells for the respective virtual circuits buffered in the buffer store 63; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39 of Gutierrez] and for forwarding said items in said particular order [switching

nodes transfer data from cells received thereby for virtual circuits on a round-robin basis, in order of virtual circuit identifier; col. 28, line 48 – col. 29, line 10 and col. 23, line 33 – col. 24, line 2 of Gutierrez]. As to the motivation for combining Gutierrez and Parruck, see the rejection to claim 23 above.

23. As to claim 34, Gutierrez as modified teaches said items correspond to packets [col. 4, lines 23 – 33 of Gutierrez and col. 7, lines 35 – 43 of Parruck].

24. As to claim 36, Gutierrez as modified teaches said items correspond to packets [col. 4, lines 23 – 33 of Gutierrez and col. 7, lines 35 – 43 of Parruck].

25. As to claim 38, Gutierrez as modified teaches said pieces of information correspond to packets [col. 4, lines 23 – 33 of Gutierrez and col. 7, lines 35 – 43 of Parruck].

26. As to claim 39, Gutierrez as modified teaches the predetermined order among the plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58 of Parruck] is a round robin order among the plurality of sub-queues [col. 28, line 48 – col. 29, line 10; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39 of Gutierrez].

27. As to claim 40, Gutierrez as modified teaches the pieces of information correspond to packets [col. 4, lines 23 – 33 of Gutierrez and col. 7, lines 35 – 43 of Parruck].

28. As to claim 41, Gutierrez as modified teaches the predetermined sequence order is a round robin order [col. 28, line 48 – col. 29, line 10; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39 of Gutierrez] among the plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58 of Parruck].

29. As to claim 42, Gutierrez teaches the enqueue distributor includes a counter for use in identifying the predetermined sequence order [buffer count value; col. 22, lines 1 – 22].

30. As to claim 43, Gutierrez as modified teaches the enqueue distributor is configured to said distribute the plurality of items among the plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58 of Parruck] without regard to the content of items of the plurality of items [col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39 of Gutierrez].

31. As to claim 49, Gutierrez as modified teaches the items correspond to packets [col. 4, lines 23 – 33 of Gutierrez and col. 7, lines 35 – 43 of Parruck].

32. As to claim 50, Gutierrez as modified teaches the sequence order among the plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58 of Parruck] is predetermined and independent of the content of said items of the stream of information [col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39 of Gutierrez].

33. As to claim 51, Gutierrez as modified teaches the predetermined order is a round robin [col. 28, line 48 – col. 29, line 10; col. 23, line 33 – col. 24, line 2 and col. 25, lines 27 – 39 of Gutierrez] among the plurality of sub-queues [VC queues 192(0) 192(k); col. 7, lines 48 – 58 of Parruck].

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONTACT INFORMATION

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on 571-272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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